AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 11, line 13 as follows:

As the frequency of the output signal 515(b) of the voltage controlled oscillator 515 increases, its edges come sooner in time (i.e., the edges advance in time). Thus, for example, the rising edges of the output signal 515(b) of the voltage controlled oscillator 515 come in better alignment with the transitions or other reference points in the data signal 565. The feedback may, therefore, ~~insure~~ ensure that the data signal and the output signal 515(b) of the voltage controlled oscillator 515 have the desired phase relationship for retiming the data via a data retimer (e.g. flip flop 470 of FIG. 4). When the desired phase relationship is reached via the feedback, then the loop may be deemed to be locked.

Please amend the paragraph beginning on page 11, line 25 as follows:

One of skill in the art will appreciate that the present invention is not limited to a particular clock and data recovery circuit. Rather the present invention is equally applicable to all clock and data ~~recover~~ recovery circuits that generate an extracted clock having a fixed phase ~~and or~~ and/or frequency relationship with a data signal. In addition, although illustrated as separate components, the present invention also contemplates different levels of integration. For example, the phase detector 560 may be integrated, at least in part, with the frequency detector 505. In addition, although many of the signals are illustrated as single-ended signals, the present invention also contemplates that some signals may be differential signals.